REMARKS / DISCUSSION OF ISSUES

The present amendment is submitted in response to the Non-Final Office Action mailed July 25, 2011.

Claim Status

Claims 1, 3-8, 14, 16-17 remain in this application. Claims 1, 3-8, 14 and 16 have been amended. In view of the amendments above and the remarks to follow, reconsideration and allowance of this application are respectfully requested. Certain Claims have been amended to remove label numbers to comport with U.S. practice.

Interview Summary

Applicants appreciate the courtesy granted to Applicant's attorney, Michael A. Scaturro (Reg. No. 51,356), during a telephonic interview conducted on Monday, October 24, 2011. Discussion turned to reasons arguments presented by Applicant's attorney distinguishing the purpose of the ramp voltage of Yamashita from the purpose of the ramp voltage of the invention. The Examiner appreciated the distinction drawn by Applicant's Attorney and suggested that claim 1 be amended to reflect the cited distinguishing features. No particular language for amending claim 1 was presented during the interview.

Information Disclosure Statement

Applicant will file an Information Disclosure Statement in compliance with 37 CFR 1.98 that reflects the search report submitted by Applicant's attorney.

Claim Objections

In the Office Action, claims 5-8 and 14 are objected to as being in improper form because a multiple dependent claim cannot depend from any other multiple dependent claim. Applicant has amended claims 3-7 and 14 in a manner which is believed to obviate the objections. Accordingly, withdrawal of the objections is respectfully requested.

Claim Rejections under 35 USC 103

The Office has rejected claims 1, 3, 4, 16 and 17 under 35 U.S.C. §103(a), as being unpatentable over U.S. Patent Application 2003/0142047 ("Inoue") in view of Japanese Patent JP-2003-241711 ("Yamashita"). Applicant respectfully traverses the rejections.

The cited portions of Inoue and Yamashita, taken individually or in any combination, fail to disclose or suggest the specific combination of claim 1. For example, the cited portions of Inoue and Yamashita fail to disclose or suggest, "*wherein the voltage on the second power supply line (50) is ramped during a pixel illumination period* ***to cancel a leakage current I_L at a gate node of the drive transistor (22) by creating a current of opposite magnitude of the leakage current I_L.***"as recited in claim 1. Emphasis added.

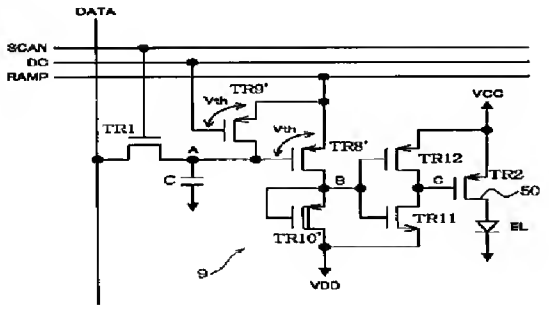
In the Office Action, it is suggested that Yamashita discloses an active matrix display device comprising an array of display pixels (drawing 1), where a power supply line is coupled to the storage capacitor (drawing 20, power supply line "RAMP" is coupled to the storage capacitor through TR8'), and wherein the voltage on the second power supply line is ramped during a pixel illumination period (drawings 20 and 21 and pars. 45-47. However, Yamashita fails to teach at least, *wherein the voltage on the second power supply line (50) is ramped during a pixel illumination period* ***to cancel a leakage current I_L at a gate node of the drive transistor (22) by creating a current of opposite magnitude of the leakage current I_L,*** as recited in claim 1.

Yamashita fails to disclose, teach or suggest the above claim limitation because Yamashita utilizes a RAMP voltage for a different purpose to yield a different result from that which is disclosed by the invention. Claim 1 has been amended to clarify this distinction. Yamashita discloses the use of a RAMP voltage for the purpose of carrying out Pulse Density Modulation of the data voltage by creating an ON-and-OFF control signal of a driver element. Yamashita creates the ON-and-OFF control signal by inputting a RAMP voltage with a predetermined variation curve to a comparison element and comparing the ramp voltage with an input data voltage. This process is described in greater detail below. In sharp contrast to Yamashita, the Applicant utilizes a RAMP voltage strictly to cancel dark currents in the phototdiode.

In Yamashita, the "RAMP" voltage is directly applied to the input of the comparator TR10', shown as element 9 in Fig. 20, shown below. When the ramp voltage rises, the difference with the DATA voltage increases in each scan period. The RAMP voltage is applied to the comparator TR10' indirectly, either through transistor TR8' or transistor TR9'. The data voltage stored on the capacitor creates a reference for the comparator TR10'. If the RAMP voltage rises, a difference with direct-current-voltage DC increases and as it exceeds the threshold level Vth between the gate sources of transistor TR8', transistor TR8' will conduct resulting in luminescence ON. As the RAMP voltage continues to rise, as it exceeds the threshold level Vth between the gate sources of transistor TR9', transistor TR9' will conduct resulting in luminescence OFF. *See* Yamashita, par. 45-47. The predetermined variation curve of the RAMP voltage determines the ON/OFF characteristic of the pixels of the display device.

Yamashita, Fig. 20:

【図２０】



In contrast to Yamashita, Applicant's Fig. 5, as shown below, illustrates an exemplary pixel layout in which capacitor Cs 24 is directly (and singly) sourced from the correction power supply line 50 (i.e., RAMP voltage) to cancel dark currents in the phototdiode 2.

Fig. 5 – showing an exemplary pixel layout of Applicant's inventive display device:

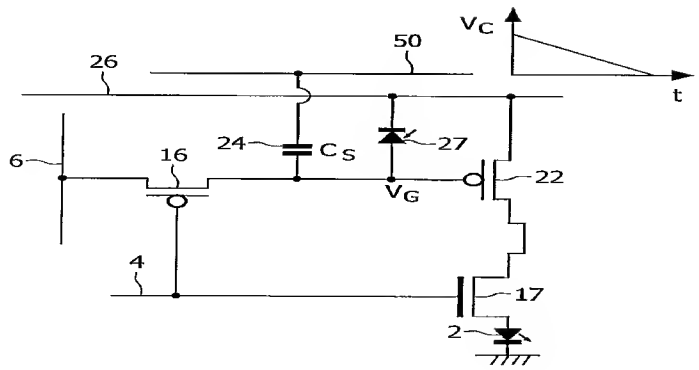


FIG.5

The light dependent device may comprise a discharge photodiode 2. The storage capacitor 24 is preferably connected between the ***gate*** of the drive ***transistor*** 22 and one of the first 26 and second 50 power lines, and the light dependent device 27 is then connected between the ***gate*** of the drive ***transistor*** and the other of the first and second power lines. Thus, the storage capacitor 24 and the photodiode 2 provide the optical feedback circuit, and these are connected between one fixed voltage line and one varying voltage line.

In accordance with the invention, the optical feedback system of the storage capacitor and the photodiode is controlled to compensate for dark currents of the photodiode. This is achieved by associating the capacitor and the photodiode with different power supply lines, and the voltage on one of the power supply lines is varied during a pixel illumination period. The effect of leakage currents on the optical feedback charging or discharging of the capacitor can then be cancelled. Applicant discloses in the Abstract, that by varying the voltage on a power supply line, the discharge characteristics of the capacitor are altered to provide compensation for the light-dependent device leakage currents. This is achieved by using the RAMP signal, i.e., a RAMP voltage supplied from the correction power supply line 50 to cancel a leakage current $I_L$at a gate node of the drive transistor (22) of opposite magnitude of the leakage current I_L, as recited in claim 1.

With reference again to Applicant's Fig. 5, shown above, the storage capacitor 24 is connected between the drive transistor gate and a second, correction, power supply line 50 which is controlled to correct for leakage (dark) photodiode currents. A correction voltage profile V_C is applied to the line 50. The currents that flow at the gate node of the drive

transistor 22 during pixel illumination (with transistor 16 off) are given by the equation:

$$-C_S \frac{dV_G}{dt} = I_{PD} + I_L \qquad [2]$$

where I_{PD} is the photo-current and I_L is the leakage current and these together equal the current that is discharging the storage capacitor 24. The leakage current shown in equation [2] is cancelled in the circuit of the invention, by creating a current at the ***gate*** node of the drive TFT ***22*** of opposite magnitude to I_L. See Applicant's published specification, pars. 54 – 60. In the simplest implementation, it can be assumed that the leakage current will be the same for every pixel in the display and that this current is constant over the frame time. By adjusting the voltage on the ***correction*** line 50 shown in FIG. 5 so that it has a constant rate of voltage change, a current at the ***gate*** of the drive TFT ***22*** can be generated so that the leakage current is cancelled. Equation [2] becomes:

$$-C_S \frac{dV_G}{dt} - C_S \frac{dV_C}{dt} = I_{PD} + I_L$$

If the rate of change of V_C is chosen correctly, then:

$$-C_S \frac{dV_C}{dt} = I_L \qquad [3]$$

Thus, the leakage current is cancelled.

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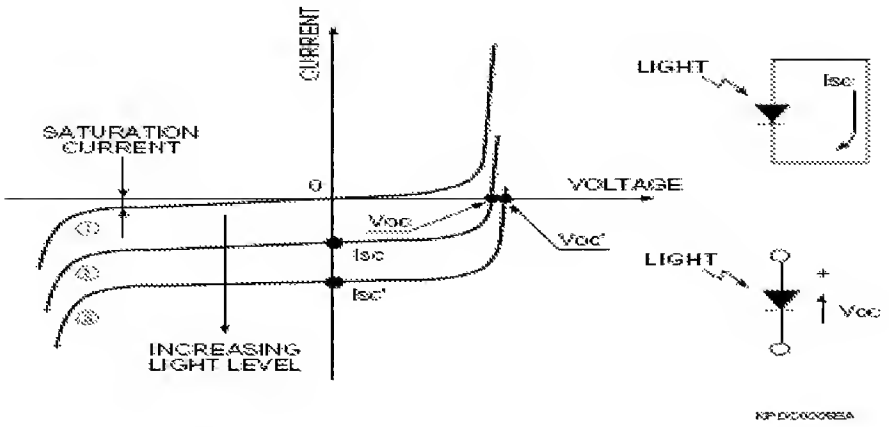
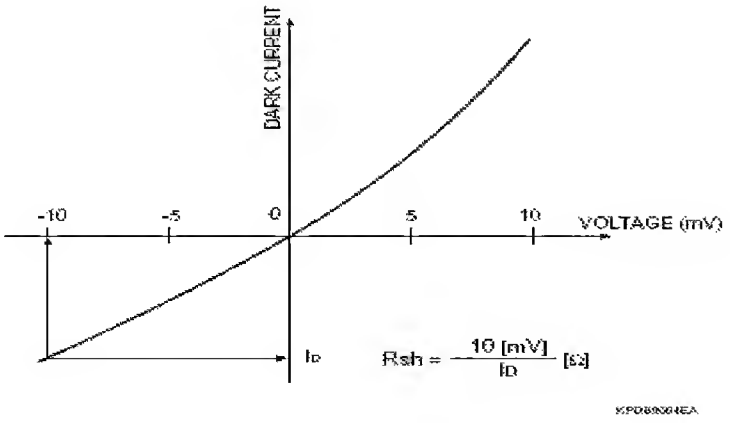
As described in par. 17 of Applicant's published application, the leakage current represents a drawback of the prior art. Leakage currents are sometimes referred to as "dark" currents. Par. 17 states that, one of the performance limiting factors for the circuits of FIGS. 3 and 4 is the leakage current through the photodiode, and this leakage current can even approach the photocurrent levels.

In general, when a voltage is is applied to a photodiode in the dark state, the current vs. voltage characteristic observed is similar to the curve of a conventional rectifier diode, shown as curve (1) in the figure below. However, when light strikes the photodiode, the

curve at (1) shifts to (2), and, increasing the amount of incident light shifts this characteristic curve still further to position (3) in parallel, according to the incident light intensity.



If the zero region of the figure above is magnified, as shown below, that the dark current ID is approximately linear in a voltage range of about ±10 mV. The slope in this region indicates the shunt resistance Rsh and this resistance is the cause of the thermal noise current.



As described above, by adjusting the voltage on the correction line 50 shown in FIG. 5 so that it has a constant rate of voltage change, a current at the gate of the drive TFT 22 can be generated so that the leakage current is cancelled, such as the one shown above is canceled.

Hence, Claim 1 is is believed to recite statutory subject matter under 35 USC 103(a). Claims 3-4 depend from independent Claim 1, which Applicants have shown to be allowable. Accordingly, claims 3-4 are also allowable, at least by virtue of their dependency from claim 1.

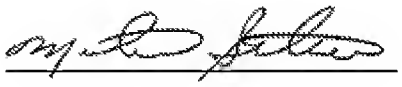
Independent Claim 16 recites similar subject matter as Independent Claim 1 and therefore contains the limitations of Claim 1. Hence, for at least the same reasons given for Claim 1, Claim 16 is believed to recite statutory subject matter under 35 USC 103(a). Claim 17 depends from independent Claim 16, which Applicants have shown to be allowable. Accordingly, claim 17 is also allowable, at least by virtue of its respective dependency from Claim 16.

Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application, namely, Claims 1, 3-8, 14, 16-17 are believed to be in condition for allowance and patentably distinguishable over the art of record.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call Mike Scaturro, Esq., Intellectual Property Counsel, Philips Electronics North America, at 516-414-2007.

Respectfully submitted,



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